Abstract

Described herein is a latch circuit (110) which has an improved maximum toggle rate or frequency. The latch circuit (110) includes a first portion (116) and a second portion (62) in which input clock signals (52,54) are applied to respective input transistors (118,78). The input transistor (118) for the first portion (116) has an emitter area which is double that of the input transistor (78) for the second portion (62). This 'imbalance' between the two input transistors (118,78) provides an increase in the 'hold period/follow period' ratio such that it is greater than 1, the self-resonance of the latch circuit (110) and also maximum toggle rate or frequency.